ABSTRACT OF THE DISCLOSURE

An input/output circuit inputs/outputs serial data. A register section comprises a first and a second register. The first register converts the serial data into parallel data. The second register converts parallel data into serial data. A first control signals supply a conversion timing for each bit when the serial data are converted into the parallel data. A second control signals supply a conversion timing for each bit when the parallel data are converted into the serial data. The signal generating circuit controls a timing of rise or fall of the first control signals and sets which of the memory cells should store a value for each bit, of the serial data, and controls a timing of rise or fall of the second control signals and sets which number of value of the serial data should be the value for each bit, of the parallel data read from the memory cells.